ments but applicable to composite devices having a MOS gate, such as a lateral IGBT. In this case, the drain is replaced with a diffusion layer having the conductivity type opposed to that of the MOS transistor. Furthermore, the present invention is effective for lateral transistors having a high withstand voltage of 100 V or more in particular. However, the present invention may also be applied to devices having a relatively low withstand voltage of 100 V or less.

**1**. A lateral semiconductor device comprising:

a support substrate,

a buried insulating film formed on said support substrate,

a first conductivity type semiconductor layer formed on said buried insulating film,

a first conductivity type first semiconductor region formed on the surface of said semiconductor layer,

a second conductivity type second semiconductor region formed in said semiconductor layer so as to be adjacent to or away from said first semiconductor region,

a second conductivity type source region formed on the surface of said first semiconductor region,

a second conductivity type drain region formed on the surface of said second semiconductor region,

a gate insulating film formed between an end of said source region on the surface of said semiconductor layer and an end of said second semiconductor region, and

a gate electrode formed on said gate insulating film, wherein

said first semiconductor region is extended from under said source region to partly under said gate electrode, the concentration distribution of a first conductivity type impurity increases in the region ranging from the surface of said semiconductor layer to said embedded insulating film and has a peak under said source region, and the impurity concentration in said semiconductor layer ranging from directly under said first semiconductor region to said embedded insulating film is lower than the surface concentration in said first semiconductor region.

**2**. A lateral semiconductor device comprising:

a support substrate,

a buried insulating film formed on said support substrate,

a second conductivity type semiconductor layer formed on said buried insulating film,

a first conductivity type well region formed so as to reach said buried insulating film from the surface of said semiconductor layer,

a first conductivity type first semiconductor region formed on the surface of said well region,

a second conductivity type source region formed on the surface of said first semiconductor region,

a second conductivity type drain region ranging formed on the surface of said semiconductor layer so as to be away from said well region,

a gate insulating film formed between an end of said source region on the surface of said semiconductor layer and an end of said well region, and

a gate electrode formed on said gate insulating film, wherein

said first semiconductor region is extended from under said source region to partly under said gate electrode, the concentration distribution of a first conductivity type impurity increases in the region ranging from the surface of said semiconductor layer to said embedded insulating film and has a peak under said source region, and the impurity concentration in said well region ranging from directly under said first semiconductor region to said embedded insulating film is lower than the surface concentration in said first semiconductor region.

**3**. A lateral semiconductor device in accordance with claim 1, wherein an interval is provided between an end of said first semiconductor region and an end of said second semiconductor region.

**4**. A lateral semiconductor device in accordance with claim 2, wherein an interval is provided between an end of said first semiconductor region and an end of said second semiconductor region.

**5**. A lateral semiconductor device in accordance with claim 1, wherein the peak of the concentration distribution of the first conductivity type impurity in said first semiconductor region is located at a depth of 0.5 μm or less from the surface of said semiconductor layer.

**6**. A lateral semiconductor device in accordance with claim 2, wherein the peak of the concentration distribution of the first conductivity type impurity in said first semiconductor region is located at a depth of 0.5 μm or less from the surface of said semiconductor layer.

**7**. A lateral semiconductor device in accordance with claim 1, wherein the surface concentration of the first conductivity type impurity in said first semiconductor region is in the range of 5 to 20% of said peak concentration.

**8**. A lateral semiconductor device in accordance with claim 2, wherein the surface concentration of the first conductivity type impurity in said first semiconductor region is in the range of 5 to 20% of said peak concentration.

**9**. A lateral semiconductor device in accordance with claim 1, wherein a first conductivity type buried region having an impurity concentration higher than that in said semiconductor layer is provided in said semiconductor layer under said first semiconductor region.

**10**. A lateral semiconductor device in accordance with claim 2, wherein a first conductivity type buried region having an impurity concentration higher than that in said semiconductor layer is provided in said semiconductor layer under said first semiconductor region.

**11**. A lateral semiconductor device in accordance with claim 1, wherein the overlap length of said first semiconductor region and said gate electrode is nearly equal to the depth of the peak of the concentration distribution of the first conductivity type impurity from the surface of said semiconductor layer.

**12**. A lateral semiconductor device in accordance with claim 2, wherein the overlap length of said first semiconductor region and said gate electrode is nearly equal to the depth of the peak of the concentration distribution of the first conductivity type impurity from the surface of said semiconductor layer.